## ABSTRACT

The invention discloses a delay-locked loop circuit with input means for a signal that is to be delayed, the input means comprising means for splitting the input signal into a first and a second branch. The signal in the first branch is connected to a component for delaying the signal, and the signal in the second branch is used as a non-delayed reference for the delay caused by the delay component in the first branch. The delay component is a passive tunable delay line, and the circuit comprises tuning means for the tunable delay line, the tuning means being affected by said reference signal, and the first branch comprises output means for outputting a delayed signal with a chosen phase delay. Suitably, the delay component is continuously tunable, for example a tunable ferroelectric delay line.